

FIG. 1

Block diagram of the LEAD3core system architecture, showing the following components and connections:

- DataRAM (104):** Connected to the CFUnit, AUnit, DUnit, and Hardware Accelerator Model (102) via a 3x16 bus.
- CFUnit (Co-processor Unit):**
 - Contains **DualMAC II copr() (108)** and **INSTRUCTION DISPATCH**.
 - Connected to **CO-PROCESSOR INSTRUCTIONS I/F (106)**.
- AUnit (Address Unit):**
 - Contains **ADDRESS GENERATION UNIT (122)** and **STATUS FLAGS**.
 - Connected to the DUnit via a 16-bit bus.
- DUnit (Data Unit):**
 - Contains **DATA ACCUMULATORS (118)**.
 - Connected to the Hardware Accelerator Model (102) via a 16-bit bus.
- Hardware Accelerator Model (102):**
 - Contains **ZA1** and **ZA2**.
 - Connected to the DUnit via a 16-bit bus.

Internal data paths within the DUnit and Hardware Accelerator Model (102) are labeled with widths: 2x40, 2, 4, 14, 116, 114, 110, 106, 151, 153, 155, and 16.

DataRAM 104

FIG. 2

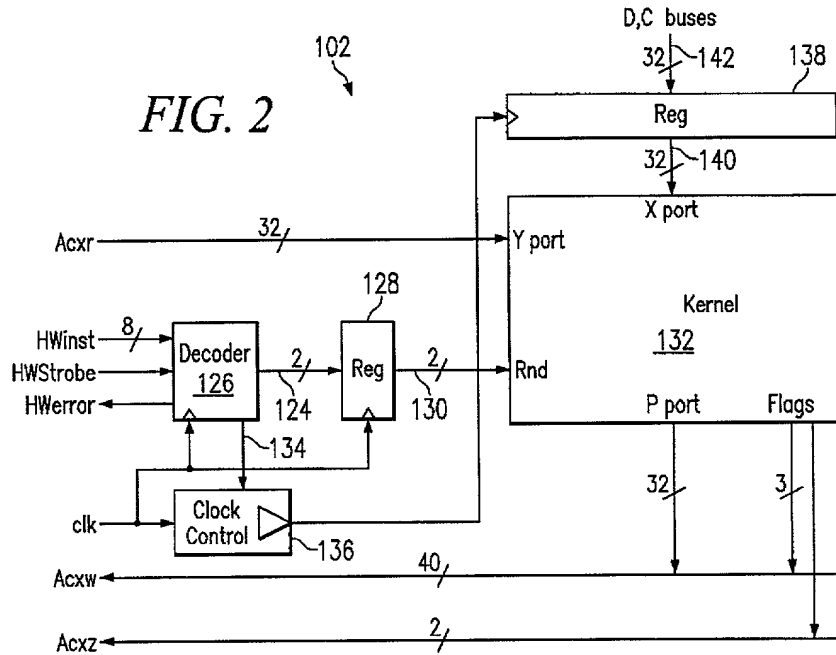
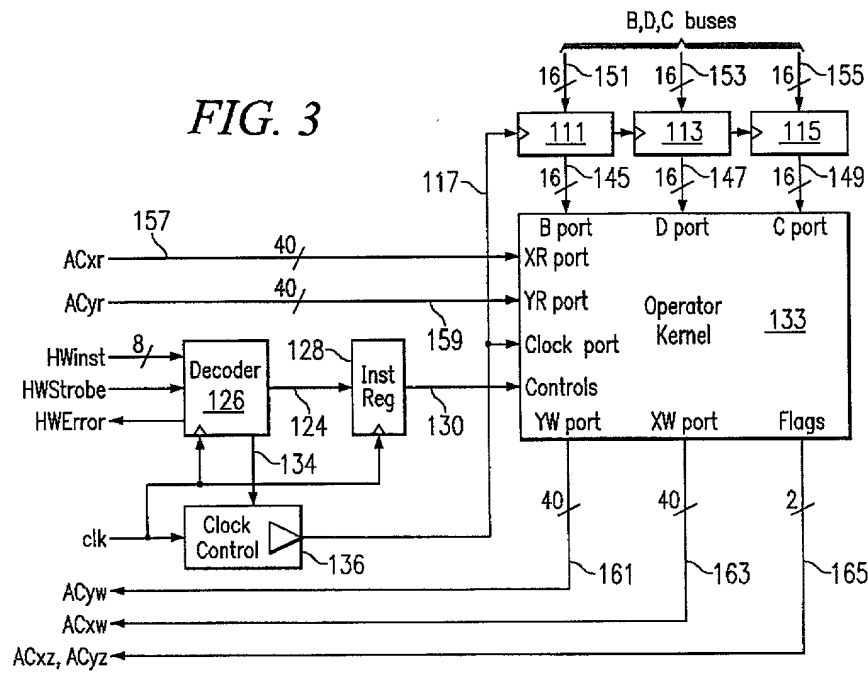


FIG. 3



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FIG. 4

The diagram illustrates the internal structure of the Operator Kernel 135. It includes a Decoder 126, an Instruction Register (Inst Reg) 128, a Clock Control block 136, and three 16-bit registers (111, 113, 115). The Decoder 126 receives HWinst (8-bit), HWStrobe, and HWError signals. The Inst Reg 128 is connected to the Controls port of the Operator Kernel. The Clock Control block 136 receives a clk signal and outputs to the Clock port of the Operator Kernel. The Operator Kernel 135 has multiple ports: B port, D port, C port, YR or XR port, Clock port, Controls, YW port, XW port, and Flags. The B, D, and C ports are connected to 16-bit registers 111, 113, and 115, which are in turn connected to B, D, and C buses. The YR or XR port is connected to a 40-bit bus. The Clock port is connected to a 40-bit bus. The Controls port is connected to a 40-bit bus. The YW port is connected to a 40-bit bus. The XW port is connected to a 40-bit bus. The Flags port is connected to a 2-bit bus. The Operator Kernel 135 outputs 40-bit signals ACy, ACx, and ACz, and 2-bit signals ACyz.

FIG. 5

The diagram illustrates the internal architecture of a digital signal processor. On the left, external inputs include **HWinst** (8-bit), **HWStrobe**, and **HWError**. These inputs feed into a **Decoder 126**. The decoder's output (124) goes to an **Inst Reg 128**. A **Clock Control** block (136) receives a **clk** signal and provides a clock signal (134) to the decoder and the instruction register. The instruction register (128) outputs (130) to the **Operator Kernel 137**. The **Operator Kernel 137** is a large block containing several ports: **B port**, **D port**, **C port**, **Clock port**, **Controls**, **YW port**, **XW port**, and **Flags**. Above the operator kernel, there are three 16-bit registers (111, 113, 115) that receive data from **B,D,C buses** (151, 153, 155) and output to the corresponding ports (145, 147, 149). The operator kernel also has three output buses: **40** (labeled 161), **40** (labeled 163), and **2** (labeled 165). These outputs are labeled **ACyw**, **ACxw**, and **ACxz, ACyz** respectively. A feedback path (117) connects the output of the operator kernel back to the input of the first 16-bit register (111).

FIG. 6

The diagram illustrates the internal architecture of a digital signal processor. Key components and their interconnections are as follows:

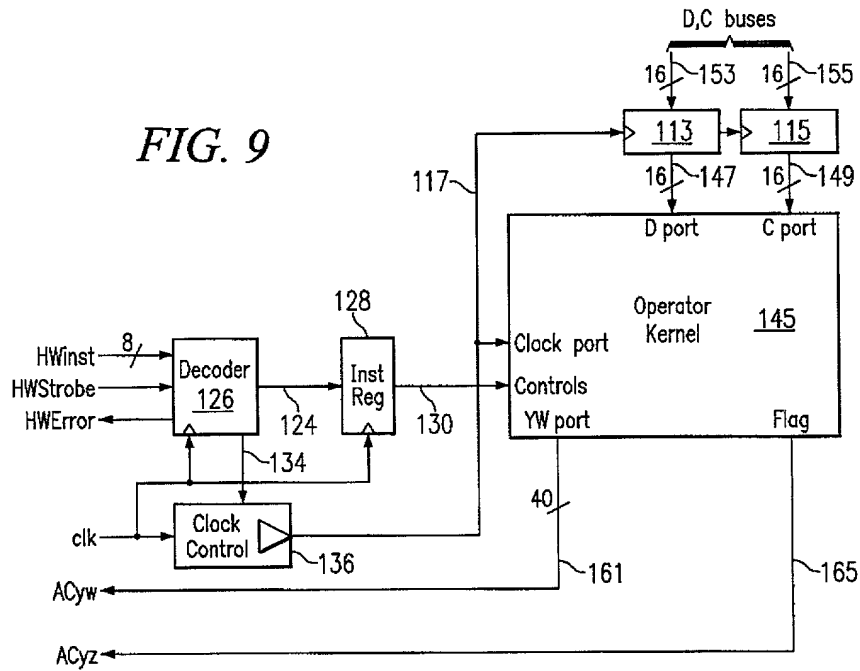
- Inputs:** ACxr (40-bit), ACyr (40-bit), HWinst (8-bit), HWStrobe, and HWEError.
- Decoder (126):** Receives HWinst and HWStrobe. It outputs an 8-bit signal to the Inst Reg (128) and a control signal (134) to the Clock Control (136).
- Inst Reg (128):** Receives the 8-bit signal from the Decoder and outputs a 1-bit signal (124) to the Controls (130).
- Clock Control (136):** Receives a clk input and outputs a clock signal (117) to the Operator Kernel (139).
- Operator Kernel (139):** The central processing unit, receiving 40-bit data from the XR port (ACxr) and YR port (ACyr), and a 40-bit clock signal (117). It outputs 40-bit signals to the XW port (ACxw) and YW port (ACyw), and a 2-bit signal to the Flags (165).
- Registers (113, 115):** Two 16-bit registers that receive data from the D port (153) and C port (155) via D,C buses. They output 16-bit signals (147, 149) to the Controls (130).
- Controls (130):** Receives control signals from the Inst Reg (124), the Operator Kernel (139), and the registers (147, 149). It outputs a 40-bit signal (161) to the XW port and a 40-bit signal (163) to the YW port.

FIG. 7

The diagram illustrates a digital signal processor (FIG. 7) with the following components and connections:

- Inputs:** ACx_r (157), HWinst (8) (8), HWStrobe, HWE_r (158), and clk.
- Internal Blocks:**
 - Decoder 126:** Receives HWinst and HWStrobe. Its output (124) goes to the Inst Reg 128 and the Clock Control 136.
 - Inst Reg 128:** Receives the output of the Decoder 126 (124) and outputs (130) to the Controls of the Operator Kernel 141.
 - Clock Control 136:** Receives clk and the output of the Decoder 126 (124). It outputs (134) to the Inst Reg 128 and (135) to the Clock port of the Operator Kernel 141.
- Operator Kernel 141:** A central block containing:
 - XR port:** Receives ACx_r (157) and outputs (117) to the D port of the D register 113.
 - Clock port:** Receives the output of the Clock Control 136 (135).
 - Controls:** Receives the output of the Inst Reg 128 (130).
 - YW port:** Outputs (161) to the ACy_w output.
 - Flag:** Outputs (165) to the ACy_z output.
- Registers:**
 - D register 113:** Receives data from the XR port (117) and outputs (147) to the C port of the C register 115.
 - C register 115:** Receives data from the D register 113 (147) and outputs (149) to the ACy_w output.
- Output Buses:**
 - ACy_w (161):** Receives data from the YW port of the Operator Kernel 141.
 - ACy_z (165):** Receives data from the Flag of the Operator Kernel 141.
- Other Labels:** 40, 153, 155, 159, 163, 167, 169, 171, 173, 175, 177, 179, 181, 183, 185, 187, 189, 191, 193, 195, 197, 199, 201, 203, 205, 207, 209, 211, 213, 215, 217, 219, 221, 223, 225, 227, 229, 231, 233, 235, 237, 239, 241, 243, 245, 247, 249, 251, 253, 255, 257, 259, 261, 263, 265, 267, 269, 271, 273, 275, 277, 279, 281, 283, 285, 287, 289, 291, 293, 295, 297, 299, 301, 303, 305, 307, 309, 311, 313, 315, 317, 319, 321, 323, 325, 327, 329, 331, 333, 335, 337, 339, 341, 343, 345, 347, 349, 351, 353, 355, 357, 359, 361, 363, 365, 367, 369, 371, 373, 375, 377, 379, 381, 383, 385, 387, 389, 391, 393, 395, 397, 399, 401, 403, 405, 407, 409, 411, 413, 415, 417, 419, 421, 423, 425, 427, 429, 431, 433, 435, 437, 439, 441, 443, 445, 447, 449, 451, 453, 455, 457, 459, 461, 463, 465, 467, 469, 471, 473, 475, 477, 479, 481, 483, 485, 487, 489, 491, 493, 495, 497, 499, 501, 503, 505, 507, 509, 511, 513, 515, 517, 519, 521, 523, 525, 527, 529, 531, 533, 535, 537, 539, 541, 543, 545, 547, 549, 551, 553, 555, 557, 559, 561, 563, 565, 567, 569, 571, 573, 575, 577, 579, 581, 583, 585, 587, 589, 591, 593, 595, 597, 599, 601, 603, 605, 607, 609, 611, 613, 615, 617, 619, 621, 623, 625, 627, 629, 631, 633, 635, 637, 639, 641, 643, 645, 647, 649, 651, 653, 655, 657, 659, 661, 663, 665, 667, 669, 671, 673, 675, 677, 679, 681, 683, 685, 687, 689, 691, 693, 695, 697, 699, 701, 703, 705, 707, 709, 711, 713, 715, 717, 719, 721, 723, 725, 727, 729, 731, 733, 735, 737, 739, 741, 743, 745, 747, 749, 751, 753, 755, 757, 759, 761, 763, 765, 767, 769, 771, 773, 775, 777, 779, 781, 783, 785, 787, 789, 791, 793, 795, 797, 799, 801, 803, 805, 807, 809, 811, 813, 815, 817, 819, 821, 823, 825, 827, 829, 831, 833, 835, 837, 839, 841, 843, 845, 847, 849, 851, 853, 855, 857, 859, 861, 863, 865, 867, 869, 871, 873, 875, 877, 879, 881, 883, 885, 887, 889, 891, 893, 895, 897, 899, 901, 903, 905, 907, 909, 911, 913, 915, 917, 919, 921, 923, 925, 927, 929, 931, 933, 935, 937, 939, 941, 943, 945, 947, 949, 951, 953, 955, 957, 959, 961, 963, 965, 967, 969, 971, 973, 975, 977, 979, 981, 983, 985, 987, 989, 991, 993, 995, 997, 999.

FIG. 9



The diagram shows the internal structure of the Operator Kernel 149. It includes a Decoder 126, an Instruction Register (Inst Reg) 128, a Clock Control block 136, and a Controls block 130. External connections are as follows:

- Inputs:** ACxr (40-bit), ACyr (40-bit), HWinst (8-bit), HWStrobe, and HWError.
- Internal Flow:** Decoder 126 outputs a 124-bit signal to Inst Reg 128. Inst Reg 128 outputs a 130-bit signal to Controls 130. A 159-bit signal also goes from Inst Reg 128 to the Controls 130. Controls 130 outputs a 117-bit signal to the Clock Control block 136. The Clock Control block 136 outputs a clock signal (clk) back to the Decoder 126.
- Outputs:** ACyw (40-bit), ACxw (40-bit), and ACxz, ACyz (2-bit).
- Other Ports:** XR port, YR port, Clock port, YW port, XW port, and Flags (2-bit).

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35	36	37	38	39	40	41	42	43	44	45	46	47	48	49	50	51	52	53	54	55	56	57	58	59	60	61	62	63	64	65	66	67	68	69	70	71	72	73	74	75	76	77	78	79	80	81	82	83	84	85	86	87	88	89	90	91	92	93	94	95	96	97	98	99	100
1	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35	36	37	38	39	40	41	42	43	44	45	46	47	48	49	50	51	52	53	54	55	56	57	58	59	60	61	62	63	64	65	66	67	68	69	70	71	72	73	74	75	76	77	78	79	80	81	82	83	84	85	86	87	88	89	90	91	92	93	94	95	96	97	98	99	100



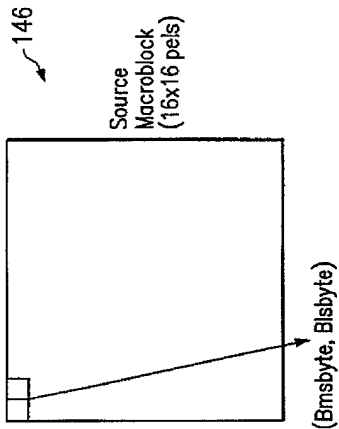


FIG. 15

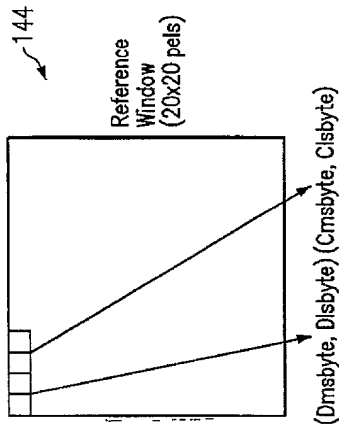


FIG. 14

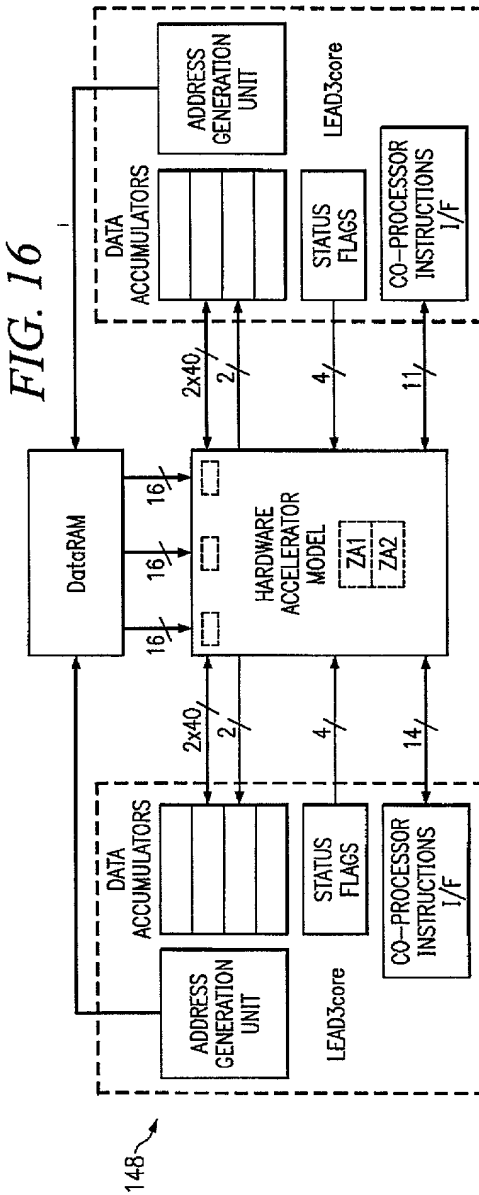


FIG. 16

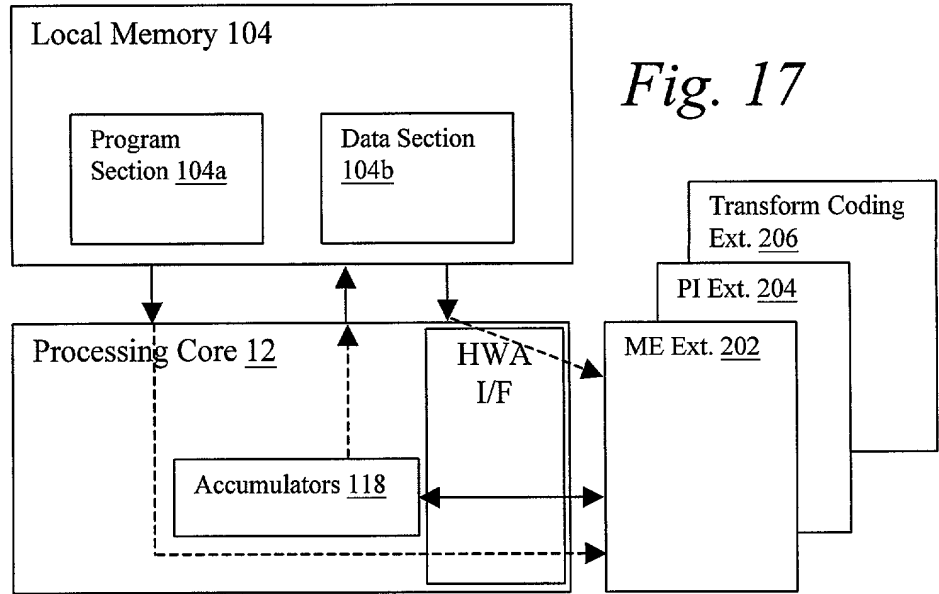
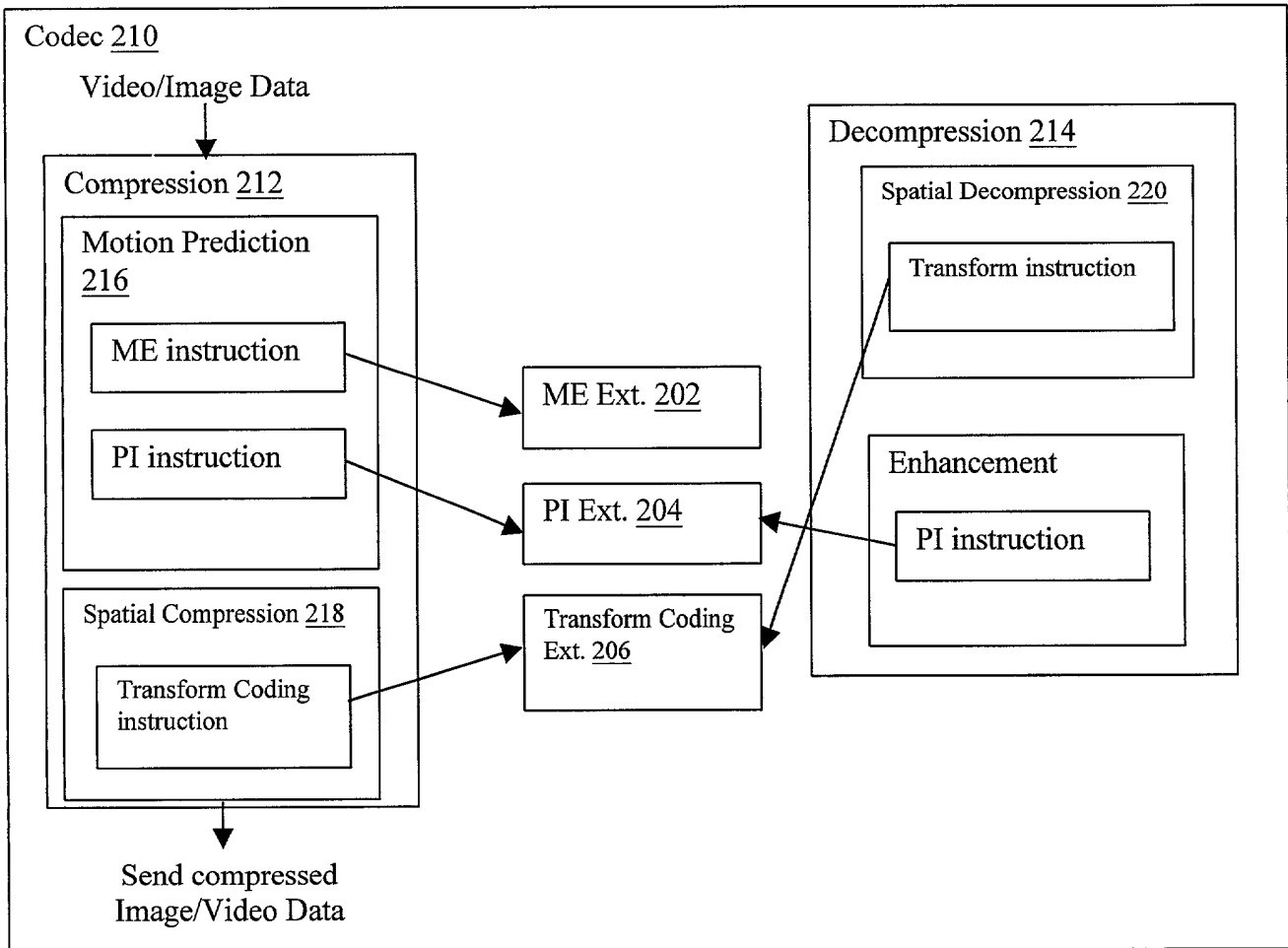


Fig. 18



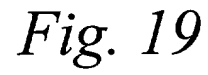


Fig. 20

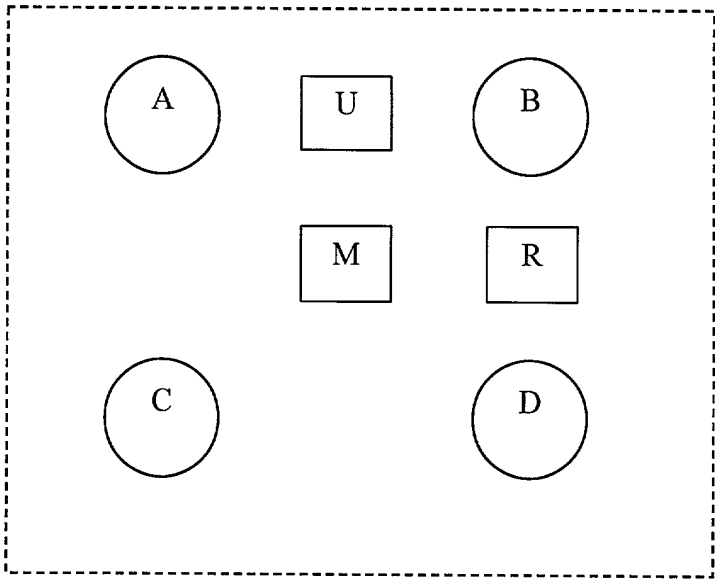
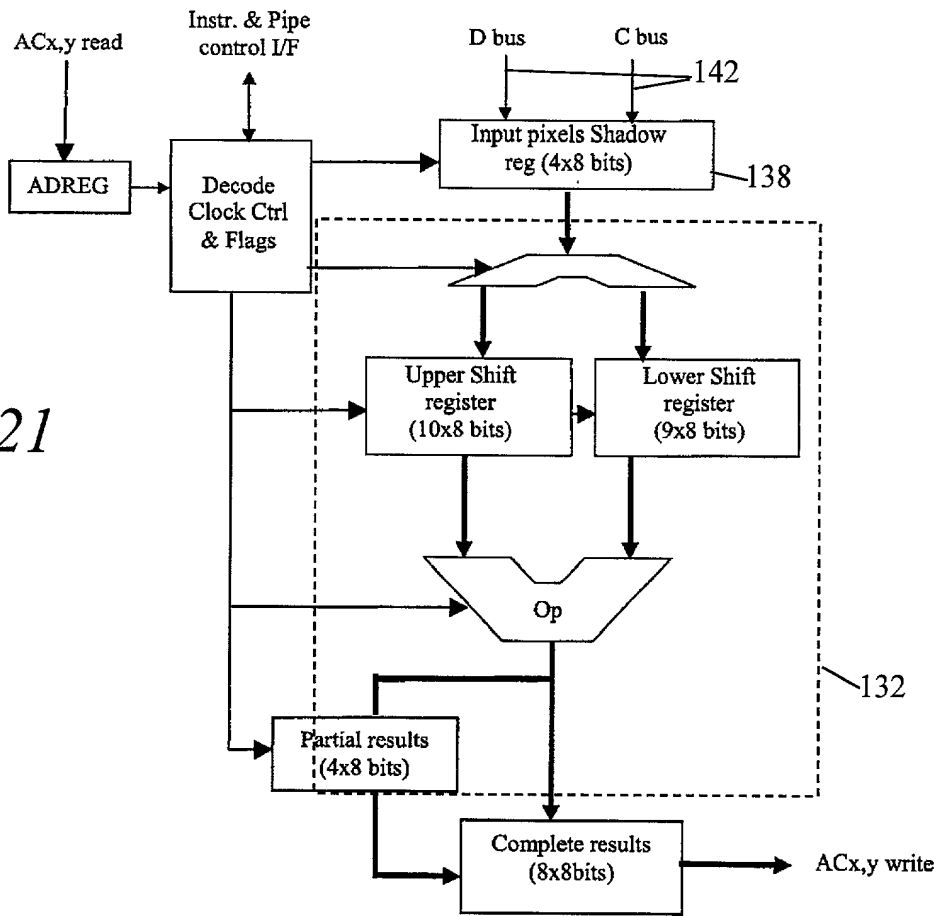


Fig. 21



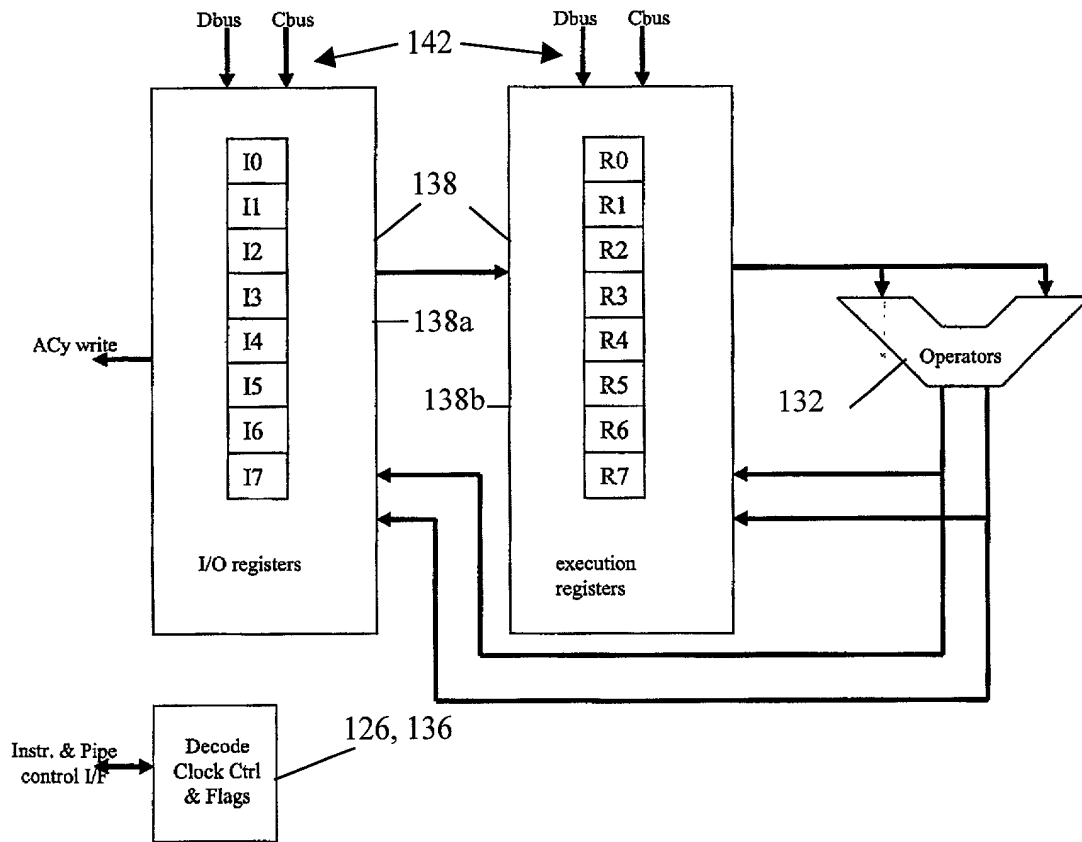


Fig. 22

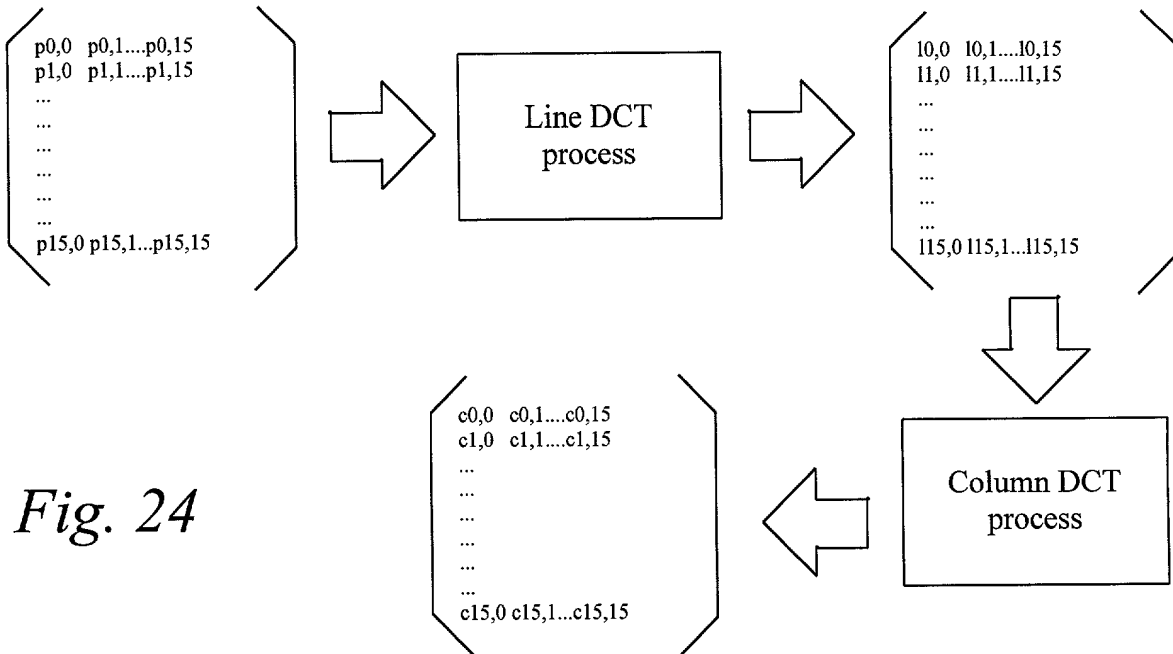


Fig. 24

